IN THE SPECIFICATION

Please amend the title of the application to read "METHOD AND APPARATUS FOR PROVIDING ~~A PROTECTED~~ PROTECTED INTELLECTUAL PROPERTY HARDWARE." In some examples, the techniques of the present invention provide one or more protected intellectual property hardware devices.

The Examiner objected to the disclosure on page 17, lines 18-20 because of informalities. Please replace the paragraph as recommended by the Examiner (page 17, line 11 – page 18, line 1) with the following amended paragraph:

For PCI applications, the typical system clock is 33 MHz or 66 MHz; for T1/E1 applications it is 8 kHz. By way of example, for 33 MHz PCI applications, and to force the IP into its protected idle state after one hour, a 47 bit protection counter C must reach a terminal count T of $30*10^9*60*60=1.08e14$. The IP owner can conceal a logic module (for example, a counter) in the IP for use in a hardware prototype. This logic module inserted by the IP owner sets a temporal hardware limitation which makes the IP provided for hardware prototype use unsuitable for production uses. In this embodiment, when the 47 bit counter reaches the value 1.08e14, the PCI IP goes into its protected idle state. This uses about 47 logic elements, covering approximately 0.3% of the area of a typical PLD ~~This are about 47 logic elements, approximately 0.3% of the area of a typical PLD~~ (for example, the APEX400 made by Altera Corp.). The PCI IP in the hardware PLD prototype board will stop working after one hour of operational run time (as counted by the hardware platform, not necessarily the total elapsed time).